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**Rasmussen, Frank Engel; Heschel, M.; Hansen, Ole**

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# Batch Fabrication of Through-Wafer Vias In CMOS Wafers for 3-D Packaging Applications

F. E. Rasmussen[1], M. Heschel[2] and O. Hansen[1]
[1]Mikroelektronik Centret, Technical University of Denmark,
Ørsteds Plads, Bldg. 345 East, DK-2800 Kgs. Lyngby, Denmark
[2]Hymite A/S, Technical University of Denmark,
Bldg. 325, 1st floor, DK-2800 Kgs. Lyngby, Denmark
E-mail: fra@mic.dtu.dk http://www.mic.dtu.dk
Phone: +45 2682 3493 Fax: +45 3927 7900

**Abstract**

A technique for fabrication of through-wafer vias in silicon wafers containing complementary metal-oxide-semiconductor (CMOS) circuitry is presented. The application of the presented through-wafer vias with existing wafer level chip size packaging (WLCSP) technologies enables fabrication of very dense packages.

The through-wafer vias are fabricated entirely by low temperature, CMOS compatible processes, thus designed to allow for post processing of vias in fully processed CMOS wafers. The fabrication of the presented through-wafer vias is based on KOH etching of wafer through-holes, low temperature deposition of dielectric material, and electrodeposition of photoresist and via metallization (Cu and Ni). A simple solution to the well-known CMOS compatibility issue of KOH is employed by protecting the front side of the CMOS wafer using a combination of plasma enhanced chemical vapor deposited (PECVD) silicon nitride, sputter deposited TiW/Au and electroplated Au. This protection scheme allows for batch processing of through-wafer vias.

The fabricated through-wafer vias have a serial resistance of 40 mΩ and a parasitic capacitance to the Si substrate of 2.5 pF.

**Introduction**

In the past few years various compact packaging technologies have been presented. State-of-the-art has moved from chip scale packages to true chip size packages fabricated on wafer level (WLCSP). [1-3] In addition the use of 3-D interconnects, in the form of through-wafer vias, has been proposed to achieve even denser packages. [4-7] Application of through-wafer via technology offers the possibility of advanced stacking of CMOS chips or stacking of various types of microcomponents directly on a CMOS chip. The latter implies the possibility of stacking e.g. MEMS-chips (MEMS for MicroElectroMechanical Systems) on CMOS chips in order to provide the often needed direct conditioning of the MEMS device output signal. A clear advantage of such a hybrid integration approach is the potential to obtain a high production yield. Through-wafer via technology also allows the interesting possibility of monolithic integration utilising the "non-active" silicon bulk of the CMOS for fabrication of e.g. MEMS devices. This integration approach can be interesting for high volume productions, though the MEMS fabrication process will be restricted by the presence of a sensitive IC circuitry and it is in general more difficult to obtain a high production yield using this integration approach.

If the concept of through-wafer vias is applied in combination with wafer level packaging, fabrication of ultra small 3-D packages containing several active devices is possible. Ultimately this 3-D package could represent a complete microsystem that could be surface mounted as a ball grid array (BGA) using solder bumps. However, a major drawback of 3-D packaging solutions is the high packaging cost mainly caused by process complexity and low yield. In recognition of this, the presented paper focuses on development of a low cost, CMOS compatible through-wafer via process. [8] The through-wafer via process is designed to be applicable as a post process to any kind of CMOS wafer regardless of the type of passivation provided by the CMOS foundry (usually silicon oxide, silicon nitride or polyimide). In order to provide CMOS compatibility the temperature must be kept low, i.e. normally below ~450°C (above this approximate temperature the CMOS Al metallization will start diffusing into the silicon, thus causing non-functional circuits). In order to allow for post processing on CMOS wafers having polyimide passivation the thermal budget is reduced even further. Thus, in present case the highest allowable process temperature has been set to 300°C.

The fabrication of the presented through-wafer vias is based on KOH etching of wafer through-holes, low temperature deposition of dielectric material, and electrodeposition of photoresist and via metallization. Utilizing the presented fabrication method single vias are obtained on the (111) surface of the wafer through-holes. Figure 1 shows a 3D illustration of a final through-wafer via.

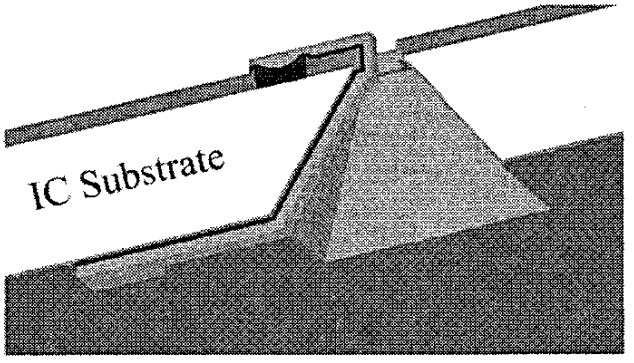


**Figure 1:** 3D illustration of final through-wafer via.

KOH etching of through-holes is chosen as an alternative to the often used deep reactive ion etching process (DRIE). [4-5] For applications needing low to medium number of vias per chip the high aspect ratio through-holes obtainable by

DRIE is not needed, and this process is therefore too costly as it does not provide the possibility of batch processing. However, KOH is not directly CMOS compatible due to ion contamination issues and the risk of causing severe damage to bonding pads (usually consisting of Al with approx. 1% Si content) and chip passivation. For this reason KOH is often disqualified for post processing on CMOS wafers. The presented through-wafer via technology employs a simple solution to this well-known CMOS compatibility issue of KOH by protecting the CMOS side of the wafer using a combination of PECVD silicon nitride, sputter deposited TiW/Au and electroplated Au. [9] This protection scheme allows for formation of through-holes in a true batch process, thereby significantly reducing the cost of the via process. Compared to a via technology based on DRIE formation of through-holes, the presented through-wafer via process offers an increased through-put due to the significant decrease in process time caused by the KOH batch process. As an illustrative example consider that 25 wafers with a thickness of 380 μm can be batch processed (through-hole etched) in approximately 5 hours using 28 wt.% KOH solution at 80°C (etch rate around 1.25 μm/min) compared to nearly 40 hours in case of DRIE of through-holes with comparable dimensions (assuming an average DRIE rate of 4 μm/min, though this etch rate will be highly dependent on feature size, etch depth, and loading).

The presented through-wafer vias are designed to accommodate the specifications set by a high-end portable product [8]; though the technology is generally applicable to applications requiring low to medium number of through-wafer interconnects per chip. In the given application only 7 through-wafer vias are needed per chip.

**Fabrication**

The through-wafer vias are processed entirely by low temperature, CMOS compatible processes. Hence, the process scheme allows for post processing of vias in any kind of fully processed CMOS wafer.

A simplified version of the process sequence is shown in figure 2. The process sequence is applied directly on the CMOS wafers as provided by the CMOS foundry (backlapped to a thickness of 380 μm).

Initially a KOH resistant silicon nitride layer is deposited on the front side of the wafer by means of plasma enhanced chemical vapor deposition (PECVD) (Figure 2-a). The CMOS wafer is then chemical mechanical polished (CMP) in order to obtain a smooth and defect free surface suitable for further processing. A KOH resistant PECVD silicon nitride layer, similar to the one previously deposited on the front side, is subsequently deposited on the backside of the wafer (Figure 2-a). On the backside the PECVD nitride is used as a KOH etch mask material and on the front side it provides a protective layer as well as a well-known surface suitable for further processing. The latter is especially important in case of polyimide passivation on the CMOS wafer. The quality of the PECVD silicon nitride is crucial to the success of the overall process. A dedicated PECVD silicon nitride process running

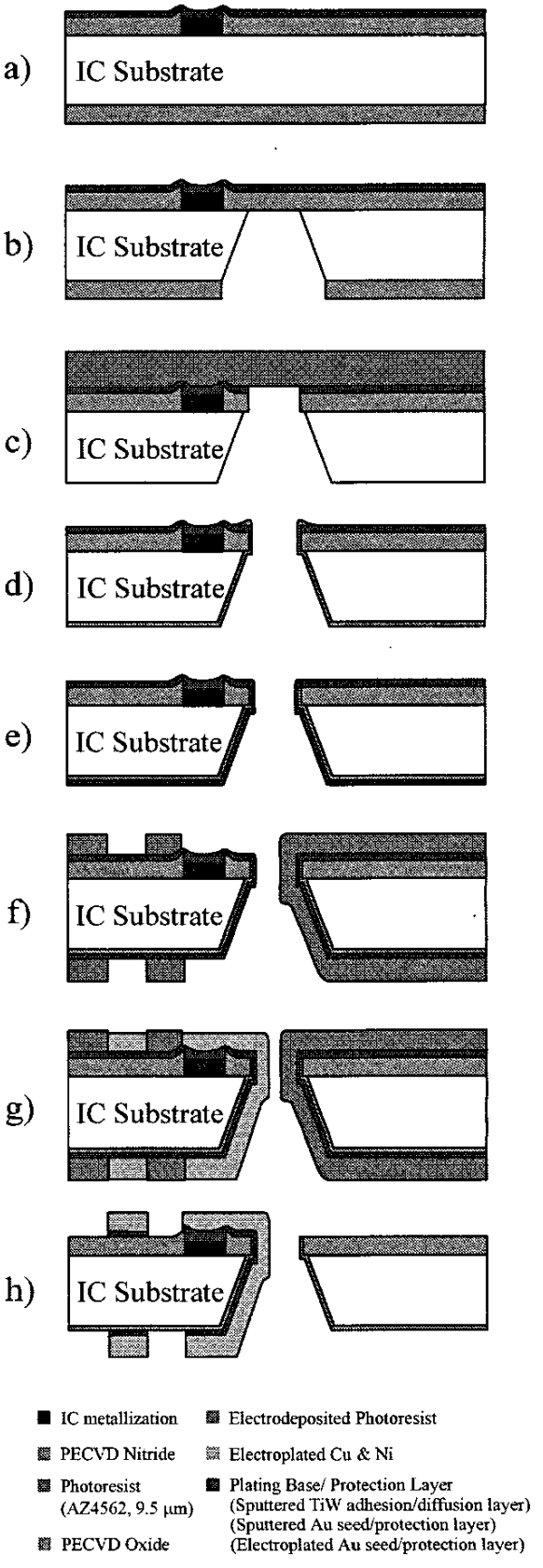


**Figure 2:** *Simplified schematic of process sequence.*

at 300°C has therefore been developed especially for this application. The developed PECVD nitride combines a low residual stress level (250 MPa compressive) with a fairly low etch rate (3 Å/min.) in 28 wt.% KOH solution at 80°C.

The PECVD nitride covering the entire front surface has to be opened above the CMOS contact pads in order to allow subsequent deposited metal layers to make electrical contact to the pads. The PECVD nitride is patterned in a reactive ion etching (RIE) process using a suitable photoresist mask.

After patterning the front side PECVD silicon nitride a metal layer consisting of 3000 Å TiW and 1500 Å Au is sputter deposited on the front side of the wafer (Figure 2-a). In combination with the previously deposited PECVD silicon nitride this TiW/Au metal layer protects the CMOS circuitry against KOH during etching of the wafer through-holes. The TiW adhesion layer has been chosen because of its low etch rate in KOH, good adhesion properties and because it provides an excellent diffusion barrier between Au and Al. [9]

Depending on the topography of the CMOS wafer surface an additional electroplated Au layer can be necessary in order to obtain sufficient protection. Electroplated coatings have the potential to yield denser coatings than obtainable by traditional microfabrication techniques and in addition the nature of the electrodeposition process ensures better coverage of complex topography. In this work a commercially available Au electrolyte (Engold 2010) has been used for this purpose. A thickness of 2.5 μm has been deposited in order to obtain a pinhole free coating. This protection scheme utilizing a combination of silicon nitride and metal layers allows for KOH etching without using a wafer holder for protection of the wafer front side. Thus, the given process enables true batch processing of wafer through-holes, which is an important feature of the presented process.

The deposited TiW/Au metal (including electrodeposited Au) serves an additional purpose besides protection. The TiW/Au layer is preserved after through-hole etching and then used as an electroplating base for deposition of via metallization in a later process step. This approach eliminates the need for an additional (and costly) metal deposition step on the front side.

The wafer through-holes are etched in 28 wt.% KOH solution at 80°C with an average etch rate of Si in the region of 1.25 μm/min. The through-hole etch is easily controlled as it self-terminates using the front side PECVD silicon nitride as an etch stop (Figure 2-b). The etch process results in creation of a layered membrane consisting of the front side PECVD nitride and the TiW/Au metal layer. In order to complete the through-hole formation this membrane has to be removed. This can be done from the front side in a photolithographic step defining the openings in a photoresist. Though in order to simplify the fabrication process, i.e. minimize the number of photolithographic steps, a maskless process for removal of the membrane has been developed. A thick layer of photoresist (9.5 μm, AZ4562) is spin coated on the front side of the wafer and immediately hard baked without exposure. Using the photoresist layer for chemical and mechanical protection of the front side the membrane can be removed from the backside of the wafer in a series of maskless etching processes (Figure 2-c). In this approach the wafer through-holes are used as a natural mask, thus defining the areas on the front side that are exposed to the etchants. The PECVD nitride is removed in an anisotropic RIE process using a gas mixture of $SF_6$ and $O_2$ (Figure 2-c). A clear end point signal can be obtained by monitoring the intensity of light emitted from excited flour atoms, $F^*$, in the plasma (done by emission spectroscopy; $F^*$ line at 703 nm). During etching of silicon nitride less flour is consumed than during etching of silicon. Hence, a corresponding shift in the $F^*$ signal from higher towards lower intensity can be observed once the nitride on the backside of the wafer (the remaining KOH etch mask) is removed and etching of silicon begins. Since the thickness of PECVD nitride on front and backside is identical the obtained end point signal can be used for determining when the nitride membranes in the bottom of the through-holes are removed.

The remaining TiW/Au membrane is subsequently removed by wet chemical etching (Figure 2-c). For TiW etching 31% $H_2O_2$ heated slightly above room temperature (32°C) is used whereas a commercial, cyanide containing etchant is used at room temperature for Au etching.

The photoresist on the front side of the wafer is stripped and a PECVD silicon oxide is deposited on the backside (Figure 2-d). The silicon oxide is needed for insulation of the final through-wafer via to the semiconductor substrate. Accordingly it is important that the PECVD silicon oxide process is capable of coating the inside of the through-holes conformably.

A metal layer consisting of TiW and Au is sputter deposited (in the given order) on top of the silicon oxide on the backside of the wafer (Figure 2-e). The sputter deposited metal is capable of coating the inside of the through-holes uniformly, and together with the previously deposited TiW/Au on the front side a perfect electroplating base is then created for subsequent electrochemical deposition of via metallization.

In order to define the structure of the via inside the wafer through-hole an electrodeposited, negatively working photoresist is applied (Eagle 2100 ED, Shipley). By applying a DC voltage across the TiW/Au electroplating base the resist is uniformly deposited all over the wafer in a cataphoretic electrodeposition process taking place at 35°C. This type of resist is not widely used within the field of MEMS, though it is well known in the printed circuit board (PCB) industry as it is originally developed for patterning of Cu wires on PCB. [10] Using a standard mask aligner the front and backside of the photoresist coated wafer is exposed through suitable photomasks defining the required structure of the mould. The electrodeposited resist is subsequently developed in a dedicated developer (Figure 2-f).

The via metallization is deposited into the photoresist mould by means of DC electroplating (Figure 2-g), which is the simplest form of electroplating. The electroplated via metallization consist of a 5 μm thick Cu layer (electrolyte: pyrophosphate Cu) capped by a thinner Ni layer (electrolyte: sulphamate Ni) for under bump metallization (UBM) and protection purposes. This metallization scheme allows for

subsequent formation of solder bumps in an organic mould (e.g. by electroplating or screen printing).

The electrodeposited photoresist mould is stripped using a dedicated remover. Finally, the underlying TiW/Au electroplating base is selectively etched to the via metallization (Figure 2-h). The TiW is etched using $H_2O_2$, whereas Au is etched using a commercial, cyanide containing etchant ensuring selectivity to Cu and Ni.

**Results & Discussion**

Figure 3 shows a SEM micrograph of through-wafer vias processed according to the presented process. The SEM micrograph shows a cross sectional view of the electroplated Cu/Ni via and circuit metallization on the backside of a wafer. The entrance of the wafer through-hole on the backside of the wafer is square with a side length of 595 μm, which corresponds to a square termination on the front side with a side length of approximately 100 μm.

As shown in Figure 3 the via metallization on the {111} sidewalls of the wafer through-hole is neatly patterned to form a single, low resistance wire. The width of the via decreases from 100 μm at the entrance of the wafer through-hole to 80 μm near the front side of the wafer. The fabricated through-wafer vias have a low serial resistance of 40 mΩ and a low parasitic capacitance of only 2.5 pF (electrical characterization has been done on dedicated test structures. The given parasitic capacitance includes contributions from two contact pads with a size of 120 μm × 120 μm). Thus, the well defined dimensions of the through-wafer vias combined with the thick metallization scheme result in an electrical

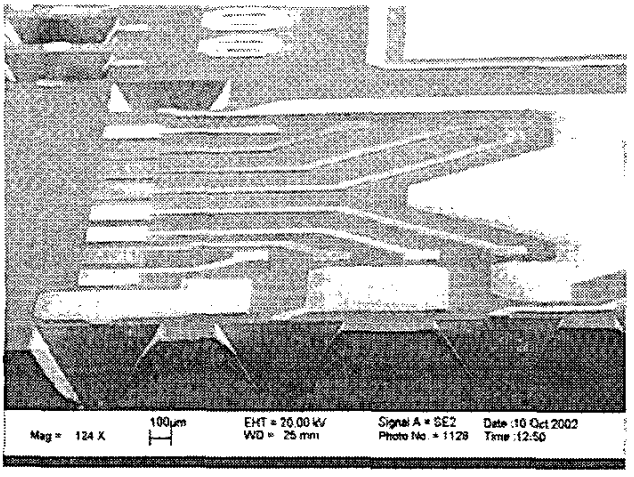


**Figure 3:** SEM micrograph of final through-wafer vias.

performance satisfying the requirements for application in modern low power, high performance electronics.

The vias have been designed to slightly decrease in linewidth in order to keep a safe distance to the neighboring sidewalls in the bottom of the through-hole and still maintain a sufficiently low serial resistance. When performing the photomask layout it is important to consider the additional effect of Fresnel diffraction (broadening of light) caused by the increasing distance between photomask and resist on the tilted (111) sidewall. This is particularly important in applications where vias with uniform linewidths are desirable. In this case compensation can simply be done by counteracting the diffraction effect by tapering the via layout on the photomask correspondingly.

Figure 4 shows a SEM micrograph of the electroplated Cu/Ni through-wafer via surrounded by the electrodeposited Eagle photoresist mould. The metallization visible on the opposing {111} sidewalls is caused by a dummy structure included in the photomask design. This dummy structure is needed in order to effectively eliminate uncontrolled light reflections inside the through-hole during exposure of the photoresist. Such light reflections are able to expose the Eagle resist beneath an otherwise masked area, thus rendering the resist in the given area insoluble in the developer and thereby leading to poorly defined dimensions of the via.

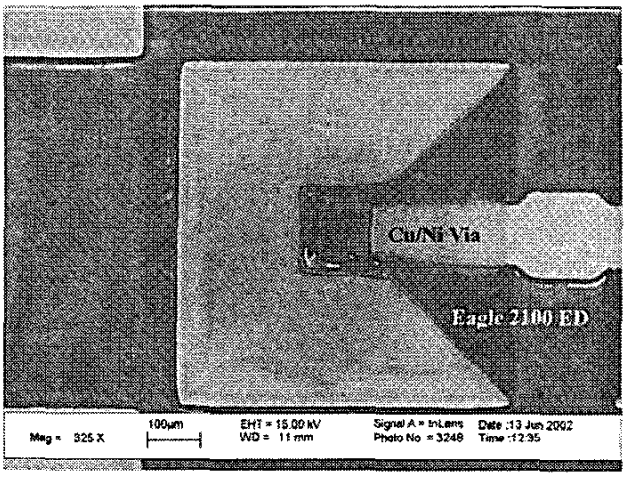


**Figure 4:** SEM micrograph showing metallization on {111} sidewalls for elimination of uncontrolled light reflections.

The through-wafer vias shown in Figure 3 lack the final passivation of the chips. The choice of material for passivation is depending on the given application of the through-wafer vias. Benzocyclobutene (BCB) and polyimide are both possible candidates for passivation. These spin-on materials are capable of coating the highly structured chip surface (i.e. including through-hole etch pits), and if a photosensitive variant of these materials are chosen openings allowing for subsequent formation of solder bumps can be defined.

Application Specific Process Modifications

An optional change to the presented process sequence is the addition of a thin Au oxidation barrier (e.g. 1000 Å) on top of the electroplated Ni. Formation of an oxide on the Ni surface can obstruct proper wetting during reflow of the solder, and furthermore decrease overall electrical performance as a thin insulating oxide is introduced in the interface between solder and UBM. Though, the thickness of the Au oxidation barrier should be carefully considered for each application as the Au is known to dissolve quickly into Sn/Pb solders. If present in high enough concentrations

formation of brittle Au-Sn compounds occurs, which adversely affects the solder joint fatigue life. [11]

According to our experiments the quality of the electroplated, reinforcing Au layer is essential for proper protection against KOH. In case of extreme topography in the region of the CMOS contact pads (in our case a 3 μm vertical step) a low quality, electroplated Au coating (e.g. with pinholes or with poor material distribution) will fail to protect the underlying pad. It can therefore be necessary to modify the process in order to improve the protection of the CMOS contact pads against KOH. In this case the protective PECVD silicon nitride has to be patterned *after* the through-hole etch, but before opening the through-holes completely (i.e. between step b and c shown in Figure 2), in order to obtain additional protection of the pads. The TiW/Au layer initially deposited on the front side therefore has to be removed after through-hole etch, thus simply making it a sacrificial layer. This adds an extra process step (sputtering) to the process sequence, as a new TiW/Au layer subsequently has to be deposited on the front side (step e, Figure 2), but in some cases this may be necessary to obtain sufficient protection of the front side of the CMOS wafer.

CMOS Compatibility

The use of sputtering for deposition of TiW/Au is a very important aspect of the presented process in order to ensure CMOS compatibility. Compared to e-beam evaporation, which is another commonly used deposition technique within microfabrication, sputtering is not associated with generation of X-rays and the risk of radiation damaging the sensitive CMOS circuitry is therefore significantly reduced (X-rays are known to cause threshold voltage shifts, etc.).

Another relevant aspect of CMOS compatibility is the formation of wafer through-holes in CMOS wafers using KOH. The presented process utilizes a protection scheme capable of protecting the CMOS contact pads against KOH, and ion contamination issues are not a problem either, as long as suitable wafer cleaning processes are used after KOH through-hole etching, e.g. Piranha cleaning (consisting of $H_2SO_4$ and $H_2O_2$ at 110°C) or RCA cleaning (a two step cleaning consisting of $NH_4OH$, $H_2O_2$, $H_2O$ and HCL, $H_2O_2$, $H_2O$ at 70°C). [12] However the performed experiments indicated problems with poor quality of the KOH etched wafer through-holes. Wafer through-holes with defects in the form of craters in {111} sidewalls and related etch mask undercut (leading to poorly defined through-holes), has been observed. The observed defects vary in size and significance.

The origin of the defects is not totally clear. One possible explanation is the presence of surface defects on the backside of the wafer. Though, the performed CMP process should deliver a planar and defect-free surface ensuring good etching results. Another possible explanation of the observed defects is related to a fundamental part of CMOS device fabrication called gettering. Gettering is the general term used for the process of moving unwanted impurities and defects from regions of the wafer that are critical to device operation to regions where they do not cause any harm. During CMOS fabrication interstitial oxygen inherently present in the silicon wafers is deliberately precipitated as silicon dioxide by high temperature treatment of the wafers. As a consequence of misfit stresses and volume change dislocations and stacking faults are generated around the precipitates. The precipitates and resulting crystal defects function as local gettering agents capable of trapping impurities, which otherwise would lead to electrical aberrations of the fabricated CMOS devices. This process is also known as intrinsic or internal gettering (for additional information on gettering see [13]). Once exposed to chemical etchants such as KOH the precipitation sites show different etch characteristic than surrounding crystal planes due to the associated crystal defects, thus causing a non-perfect KOH etch pit with cratered sidewalls. Depending on the initial concentration of interstitial oxygen this problem can be more or less pronounced. [14] In general for applications involving bulk silicon micromachining in CMOS wafers, it can therefore be recommended to use silicon wafers with a low interstitial oxygen concentration as a starting material for the CMOS device fabrication. Though, this requires a modified gettering technique, where e.g. an external sink for gettering of impurities can be provided by a thin film such as polysilicon on the backside of the wafer. This type of gettering is known as extrinsic gettering. However, not all CMOS foundries provide this technology.

## Conclusions

The through-wafer vias are an ideal tool for achieving denser packages as they allow for integration of microcomponents with integrated circuitry through monolithic as well as hybrid integration approaches.

The presented process allows for batch fabrication of through-wafer vias in wafers containing sensitive CMOS circuitry. The fabricated through-wafer vias have a low serial resistance of 40 mΩ and a low parasitic capacitance to the Si substrate of 2.5 pF.

Wafer through-holes with cratered {111} sidewalls and related etch mask undercut have been observed. It has not been possible to determine the exact origin of these defects. Though, the silicon material used for CMOS device fabrication is essential to the through-wafer via process. In order to obtain well defined wafer through-holes by KOH etching the bulk of the CMOS wafer needs to be free of heavy crystal defects. In this sense the quality of the bulk silicon depends on the initial concentration of interstitial oxygen in the silicon wafers used for CMOS device fabrication. For applications requiring post processing of through-wafer vias it is therefore advisable to consider the use of CMOS technology fabricated on silicon with an initial low interstitial oxygen concentration, and if possible fabricated using extrinsic gettering.

Future KOH etch experiments are planned to investigate the issue of non-perfect formation of wafer through-holes in CMOS wafers.

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